wherein said semiconductor chips and said spacer members are stacked alternately such that said electrodes of said semiconductor chips directly contact corresponding conductive patterns at a portion of the corresponding conductive patterns formed on the surface of the spacer member and are electrically connected to said conductive patterns of said spacer members, and said conductive patterns of said spacer members are electrically connected to each other.

SEE APPENDIX FOR CHANGES MADE TO CLAIM 14

REMARKS

Claims 14-16 stand rejected under 35 U.S.C. § 102 as being anticipated by Akram et al. and Sugano et al.. This rejection is respectfully traversed for the reasons discussed in the response filed June 3, 2002. Nevertheless, in order to expedite prosecution, claim 14 has been amended to clarify the distinction between the present invention and the cited prior art.

As a preliminary matter, it is submitted that both Akram et al. and Sugano et al. are directed to stacking completed packages, whereas the present invention stacks separated chips 7 and spacers 12 as shown in Figures 17-20. Accordingly, the cited prior art does not disclose "wherein said semiconductor chips and said spacer members are stacked alternately ... " as recited in claim 14. In contrast, both Akram et al. and Sugano et al. disclose ***completed packages*** which include the chip and alleged spacer ***as a unitary structure*** which can not be separated to be stacked ***alternatively*** as recited in claim 14. That is, the cited prior art does not disclose or suggest stacking alternately a chip and a separate spacer, but rather, the cited prior art discloses stacking completed semiconductor packages as a whole.

Further, neither Akram et al. nor Sugano et al. disclose or suggest "said electrodes of said semiconductor chips ***directly contact*** corresponding conductive patterns at a portion of the corresponding conductive patterns ***formed on the surface of the spacer member***" as recited in claim 14. For example, Sugano et al. discloses that the alleged electrodes 304 contact a portion of the alleged conductive pattern 308 which is NOT concurrently formed ***on the surface*** of the alleged spacer member 310, 314. That is, lead 308 extends away and is separated from the alleged spacer members 310, 314. Similarly, in Akram et al., the alleged electrodes 24 directly contact an intermediate bond wire 22 which couples the electrode to the alleged conductive pattern 26, rather than being directly connected to any portion of the conductive pattern itself (let alone a portion formed on the surface of the alleged spacer). Accordingly, both Akram et al. and Sugano et al. form ***indirect*** connections between the electrodes and the portion of the conductive pattern formed on the spacer, whereas the present invention defines electrodes that are directly connected to the conductive patterns.

The aforementioned distinctions underscore the general difference between the present invention as recited in claim 14 and the cited prior art. Namely, the present invention enables a ***direct*** electrical connection between the separated chip and conductive patterns in a compact, simple design whereby the spacer and chip are alternating; rather than the indirect, convoluted connections in the completed unitary packages of Akram et al. and Sugano et al..

Based on the foregoing, it is submitted that claims 14-16 are patentable over Akram et al. and Sugano et al.. Accordingly, it is respectfully requested that the rejection of claims 14-16 under 35 U.S.C. § 102 over Akram et al. and Sugano et al., be withdrawn.

CONCLUSION

Having fully and completely responded to the Office Action, Applicants submit that all of the claims are now in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,
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APPENDIX

14. (Amended) A semiconductor device comprising:

a plurality of semiconductor chips each having electrodes formed on the major surface thereof, and

a plurality of spacer members each having a conductive pattern on the surface thereof;

wherein said semiconductor chips and said spacer members are stacked alternately such that said electrodes of said semiconductor chips directly contact corresponding conductive patterns at a portion of the corresponding conductive patterns formed on the surface of the spacer member and are electrically connected to said conductive patterns of said spacer members, and said conductive patterns of said spacer members are electrically connected to each other.